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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/538,684	03/30/2000	Larry D. Kinsman	3056.1US (96-803.1)	8722
7590 06/15/2005			EXAMINER	
Joseph A Walkowski Trask Britt & Rossa P O Box 2550 Salt Lake City, UT 84110			GRAYBILL, DAVID E	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/538,684

Applicant(s)

KINSMAN ET AL.

Examiner

David E. Graybill

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4, 6-12, 14-29, 31-37 and 39-45 is/are pending in the application.
- 4a) Of the above claim(s) 7, 21, 23 and 32 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 8-12, 14-20, 22, 24-29, 31, 33-37 and 39-45 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 1 page.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

In the rejections *infra*, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4, 6, 8-12, 14-20, 24-27, 29, 31, 33-37 and 39-45 are rejected under 35 U.S.C. 102(b) as anticipated by Marrs (5701034) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Marrs.

At column 1, lines 37-44; column 2, lines 33-42; column 3, lines 34-40; column 4, lines 6-16; column 5, lines 1-33; column 5, line 67 to column 6, line 23; column 6, lines 59-61; column 8, lines 63 and 64; column 10, lines 17, 18, 24 and 42-46; and column 11, lines 35 and 36, Marrs teaches the following:

1. An integrated circuit package inherently having reduced inductance comprising: a package body 120; an integrated circuit die 101 positioned within the package body; a lead frame including a plurality of leads 102 having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; and an electrically conductive heat sink 110 positioned at least partially within the package body with a surface 110b of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second

portion of the heat sink 110a under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

2. The integrated circuit package of 1, wherein the package body includes one of a transfer molded plastic package body and a preformed ceramic package body.

4. The integrated circuit package of 1, wherein the lead frame includes one of a peripheral-lead finger lead frame, a Leads Over Chip lead frame, and a Leads Under Chip lead frame.

6. The integrated circuit package of 1, wherein the heat sink is coupled to the reference voltage through one of a wirebond 117, a conductive adhesive, and a welded connection.

8. The integrated circuit package of 1, wherein the heat sink is positioned only partially within the package body (surface 110a is externally exposed).

9. The integrated circuit package of 1, wherein the heat sink is coupled to a printed circuit board outside the package body thereby coupled (by leads 102) to one of a signal voltage and a reference voltage.

10. The integrated circuit package of 8, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

11. The integrated circuit package of 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

12. The integrated circuit package of 1, wherein the heat sink is positioned within the package body with its first portion extending i substantially to at least one side of the package body.

14. The integrated circuit package of 1, wherein the first and second portions of the heat sink are integral with one another.

15. The integrated circuit package of 1, wherein the first and second portions of the heat sink comprise separate parts.

16. The integrated circuit package of 1, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

17. The integrated circuit package of 1, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

18. The integrated circuit package of 1, wherein the heat sink has locking holes 112 therein for locking the heat sink in the integrated circuit package.

19. The integrated circuit package of 1, further comprising an adhesive 118 attaching the lead frame to the heat sink.

20. The integrated circuit package of 1, wherein the integrated circuit package comprises one of a Vertical Surface Mount Package, a Small Outline J-lead package, a Thin Small Outline Package, a Quad Flat Pack, and a Thin Quad Flat Package.

24. An integrated circuit package inherently having reduced lead inductance comprising: a package body; an integrated circuit die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; and an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion (rim/periphery/edge), said columnar portion having a vertical thickness which is greater than the vertical thickness of said skirt portion, and having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment

surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body, the die-attach surface being attached to the integrated circuit die.

25. An integrated circuit package inherently having reduced lead inductance comprising: an integrated circuit die; a lead frame including a plurality of leads having portions that are connected to the integrated circuit die, the plurality of leads forming an area; and an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of an enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

26. The integrated circuit package of 25, further comprising a package body.

27. The integrated circuit package of 26, wherein the package body is selected from a group consisting of a transfer molded plastic package body and a preformed ceramic package body.

29. The integrated circuit package of 25, wherein the lead frame is selected from a group consisting of a peripheral-lead finger lead frame, a Leads Over Chip lead frame, and a Leads Under Chip lead frame.

31. The integrated circuit package of 25, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

33. The integrated circuit package of 26, wherein the heat sink is positioned only partially within the package body.

34. The integrated circuit package of 26, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

35. The integrated circuit package of 34, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

36. The integrated circuit package of 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

37. The integrated circuit package of 26, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

39. The integrated circuit package of 25, wherein the first and second portions of the heat sink are integral with one another.

40. The integrated circuit package of 25, wherein the first and second portions of the heat sink comprise separate parts.

41. The integrated circuit package of 25, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

42. The integrated circuit package of 25, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

43. The integrated circuit package of 25, wherein the heat sink has locking holes therein for locking the heat sink in the integrated circuit package.

44. The integrated circuit package of 25, further comprising an adhesive attaching the lead frame to the heat sink.

45. The integrated circuit package of 25, wherein the integrated circuit package comprises one of a Vertical Surface Mount Package, a Small Outline J-lead package, a Thin Small Outline Package, a Quad Flat Pack, and a Thin Quad Flat Pack.

To further clarify the disclosure of the package inherently having reduced lead inductance, it is noted that the term "reduced" is a relative term of degree, and it is inherent that the package has a reduced lead inductance relative to any greater inductance. In any case, although Marrs does not appear to explicitly disclose the process/intended use limitation "having a reduced lead inductance," the product of Marrs inherently possesses any structural characteristics imparted by the process limitation. See *In re Fitzgerald, Sanders, and Bagheri*, 205 USPQ 594 (CCPA 1980).

To further clarify the teaching of said columnar portion having a vertical thickness which is greater than the vertical thickness of said skirt portion, it is noted that the columnar portion has a vertical thickness

between 110b and 112 which is greater than the vertical thickness of the skirt portion between 112b and 112a.

To further clarify the teaching of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body, it is noted that it is inherent that a first portion of the heat sink facing the lead frame is in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body because Marrs teaches that a first portion of the heat sink facing the lead frame is very near to a substantial part of the enclosed portion of all (100 percent) of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body.

In any case, because applicant insists on unique interpretations of the disclosure of Marrs, and to continue to afford applicant the benefit of compact prosecution, in the alternative, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular area percentage, and columnar portion and skirt relative

thicknesses because applicant has not disclosed that the percentage and thicknesses are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the product would possess utility using other dimensions. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Also, although Marrs does not appear to explicitly disclose "for reducing lead inductance during the operation of the integrated circuit die positioned within the package when compared to that of a conventional, grounded heat sink," this statement of intended use of the product does not result in a structural difference between the claimed product and the product of Marrs. Further, because the product of Marrs has the same structure as the claimed product, it is inherently capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed product from the product of Marrs. The manner in which a product

operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof [here content of inductance] during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Claims 3, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marrs as applied to claims 1, 2, 4-6, 8-20, 24-27, 29-31 and 33-45, and further in combination with Wark (5696031).

Marrs does not appear to explicitly teach the following:

3. The integrated circuit package of 1, wherein the integrated circuit die includes one of a Dynamic Random Access Memory integrated circuit die, a Static Random Access Memory integrated circuit die, a Synchronous Dynamic Random Access Memory integrated circuit die, a Sequential

Graphics Random Access Memory integrated circuit die, a flash Electrically Erasable Programmable Read-Only Memory integrated circuit die, and a processor integrated circuit die.

22. An electronic system comprising an input device, an output device, a memory device, and a processor device coupled to the input, output, and memory devices, at least one of the input, output, memory, and processor devices including an integrated circuit package comprising: a package body; an integrated circuit die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; and an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body and having a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink and the integrated circuit die.

28. The integrated circuit package of 25, wherein the integrated circuit die is selected from a group consisting of a Dynamic Random Access Memory integrated circuit die, a Static Random Access Memory integrated circuit die, a Synchronous Dynamic Random Access Memory integrated circuit die, a Sequential Graphics Random Access Memory integrated circuit die, a flash Electrically Erasable Programmable Read-Only Memory integrated circuit die, and a processor integrated circuit die.

Nonetheless, at column 5, lines 59-65, Wark teaches these limitations. Moreover, it would have been obvious to combine the product of Wark with the product of Marrs because it would provide an electronic system.

Applicant's amendment and remarks filed 3-21-5 and 9-1-4 have been fully considered, and are addressed by the rejection *supra*, or previously have been adequately addressed in the record.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will

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expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**For information on the status of this application applicant should check PAIR:**

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**Alternatively, applicant may contact the File Information Unit at (703) 308-2733.**

**Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.**

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.  
The fax phone number for group 2800 is (703) 872-9306.



David E. Graybill  
Primary Examiner  
Art Unit 2822

D.G.  
9-Jun-05